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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/241,695 | 02/02/1999 | AKIHARU MIYANAGA | SEL123 | 9049 |

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| EXAMINER |
|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 07/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/241,695 | MIYANAGA ET AL. | |
| | Examiner | Art Unit | |
| | Shouxiang Hu | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,5-13,15-48 and 50-59* is/are pending in the application.

4a) Of the above claim(s) *5-13,16,17,19,20,22,23,25,26,35-41 and 50-55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,15,18,21,24,27-34,42-48 and 56-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a) because Fig. 8 fails to show the detail of the impurity distributions as that shown in Fig. 3. According to the specification (page 15), the impurity region 804 is added after the gate is formed. Accordingly, the impurity region should be substantially uneven in the region under the gate, because of the shadow effect of the gate. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

2. Claims 42-48 are objected to because of the following informalities and/or defects:

In claim 42, the term of "not in contact with the drain region" should read as: --not in contact with the first drain region--.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 57 recites the limitations "the first n-type impurity", "the second n-type impurity" and "the first and the second p-type impurity(ies)." There is insufficient antecedent basis for each of those limitations in the claim.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 15, 18, 21, 24, 27-34 and 42-48, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr et al. ("Burr"; US 5,650,340).

Burr discloses a semiconductor device having a MOSFET (Fig. 5; col. 14, lines 22-36), comprising: source and drain regions (136 and 138; n+) with a first impurity; a channel forming region (144) between the source and drain regions; an impurity region (147; p+) including a second impurity having a conductive type opposite to that of the source and drain regions, wherein the impurity region (147) is formed under the channel forming region and in the source region (see the similar p+ region 116 in Fig. 4G) and not in contact with the drain region; and a pair of LDD regions (136A and 138A). Burr

further discloses that the channel forming region can have a doping concentration of $1x10^{14}$ /$cm^3$ through $1x10^{16}$ /$cm^3$ (see col. 5, lines 29-33) and the impurity region can have a doping concentration of $1x10^{17}$ /$cm^3$ through $1x10^{18}$ /$cm^3$ (see col. 6, lines 21-30), which naturally covers a concentration ratio that is between 1/100 and 1/10.

Regarding claims 1, 15, 18, 21, 24, 27-34, although Burr does not expressly disclose that the semiconductor device can have a plurality of above MOSFET, one of ordinary skill in the art would readily recognize that a semiconductor device normally integrates plurality of individual MOSFETs in order to form an integrated circuit with desired functionality.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make Burr's semiconductor device comprising the MOSFET with a plurality of the individual MOSFETs being integrated, so that an integrated circuit with desired functionality would be obtained.

Regarding claims 42-48, Burr further discloses that the MOSFET can be used in CMOS (see col. 14, line 65, through col. 15, line 47) and that the MOSFET can be either a p-channel type or an n-channel type (see col. 11, lines 57-67, and col. 15, lines 63-64). Although Burr does not explicitly disclose that such types of p-channel MOSFET and n-channel MOSFET can be used to form a CMOS circuit, one of ordinary skill in the art would readily recognize that CMOS structure is one of the most common basic structures in an IC device for achieving advanced functionality with reduced power consumption, and that a CMOS structure can be readily formed with an n-channel

MOSFET and a p-channel MOSFET having a polarity opposite to that of the n-channel MOSFET.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a p-channel MOSFET having a reverse polarity to the n-channel MOSFET of Burr into the semiconductor device of Burr, so that a CMOS semiconductor device having advanced functionality with reduced power consumption would be achieved.

Regarding claims 18, 21, 24, 29-33 and 45-47, it is noted that it is old and well known in the art that semiconductor devices having MOSFETs with short channels can be used in various well-known devices with different functionalities, including microprocessors (such as RISC or ASIC ones), cellular phones, personal handy phone systems and portable computers (as evidenced in the prior art references such as Rostoker et al. (US 5,563,928; see co.3, lines 52-58) and Okumura et al. (US 5,945,972; see col. 2, lines 15-21)). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the semiconductor device of Burr and to use it in the above well-known devices for achieving desired device functionalities with improved performance.

Regarding claim 27, 34 and 48, it is noted that one of ordinary skill in the art would readily recognize that the impurity region can be formed at a depth of about 20 nm or deeper in order to maintain high mobility in the channel-forming region, as evidenced in the prior art such as Burr (US 6,093,951; see col. 8, lines 24-31).

Regarding claim 28, it is noted that the MOSFET in Burr is a bulk MOSFET formed on a silicon substrate, and one of ordinary skill in the art would readily recognize that such a silicon substrate with the bulk MOSFET device is commonly formed of a single crystal silicon wafer.

Regarding claim 43, it is noted that Ar and P are the two most commonly used n-type impurities (see col. 12, lines 1-4 in Burr), born is most commonly used p-type impurity in the industry (see col. 11, lines 60-63).

6. Claims 56-59, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Burr et al. ("Burr"; US 5,650,340), as applied to claims 1, 15, 18, 21, 24, 27-34 and 42-48, in view of Hook et al. ("Hook"; US 6,083,794), Mikoshiba (JP 56060061 A) and/or Okumura et al. ("Okumura"; US 5,945,972).

The disclosure of Burr is discussed as applied to claims 1, 15, 18, 21, 24, 27-34 and 42-48 above.

Burr further discloses that the second impurity for the impurity region can be injected through an angled implantation (see col. 14, lines 33-36). Although Burr does not expressly disclose that the implantation angle can be about 45 degrees, one of ordinary skill in the art would readily recognize that a 45-degreee implantation angle is well within the commonly recognized range for angled implantation with desired implantation profile, as evidenced in Hook (see the implantation angle of substantially about 45 degrees to the vertical in Fig. 2 for the impurity region 46 in Fig. 3). And, it is

noted that the exact impurity injection direction is an art-recognized parameter of importance subject to routine experimentation and optimization.

In addition, although Burr does not expressly disclose that the channel is oriented along a <100> direction, one of ordinary skill in the art would also readily recognize that the channel in a MOSFET can be desirably aligned to a <100> crystal direction on a wafer parallel to a (100) crystal plane for minimizing the adverse piezo effect, as evidenced in Mikoshiba (Fig. 1), which comprises a gate (5) aligned along a {100} direction on a (100) substrate. With the impurity injection direction being about 45-degrees to the vertical and the channel being aligned along a <100> direction, the impurity injection direction would be inherently along a <110> direction.

Furthermore, although Burr does not expressly disclose that the MOSFET device can be used as an EL display device, one of ordinary skill in the art would readily recognize that a MOSFET can be readily used in EL display units having an actively-addressed structure for good display quality, as evidenced in Okumura (see col. 28, lines 14-11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the above semiconductor device of Burr with the implantation angle being about 45 degrees, with the channel being aligned to a <100> crystal direction on a wafer parallel to a (100) crystal plane, and with the MOSFET being applied to an EL display device, as taught in Hook, Mikoshiba and/or Okumura, so that a desired EL display device with desired implantation profile and minimized piezo effect would be achieved. And, in such a collectively taught device, the impurity injection

direction would be about 45-degrees to the vertical and the channel would be aligned along a <100> direction; thus the second impurity injection direction would be naturally along a <110> direction, which would then be inherently perpendicular to a plane having the smallest atomic density of the semiconductor substrate.

### *Response to Arguments*

7. Applicant's arguments with respect to claims 1, 15, 18, 21, 24, 27-34, 42-48 and 56-59 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References C and D are cited as being related to a MOSFET structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703) 306-5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SH
July 8, 2003

Shouxiang Hu
Patent Examiner
TC2800